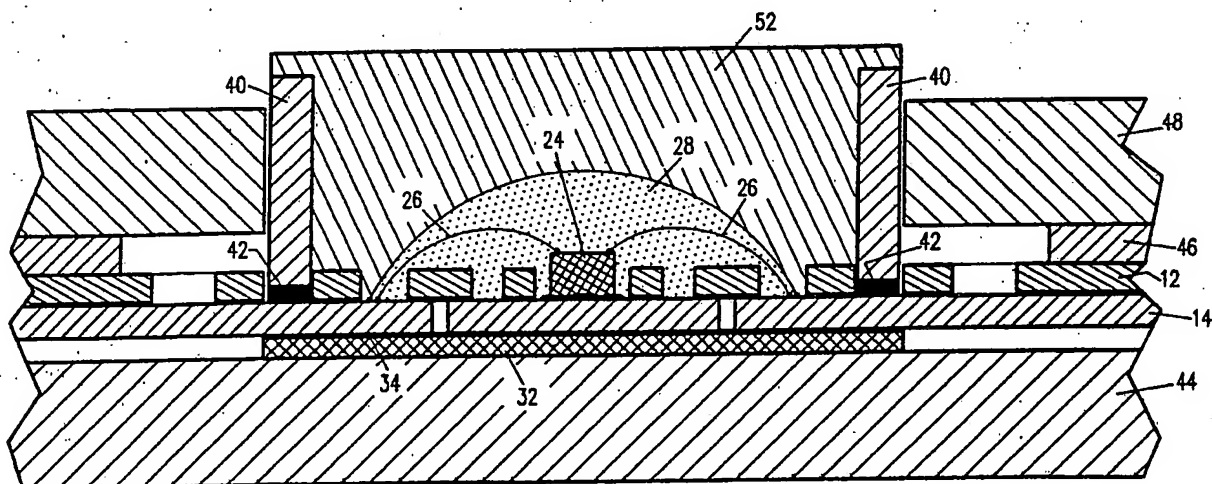




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<p>(21) International Application Number: PCT/US88/03790</p> <p>(22) International Filing Date: 26 October 1988 (26.10.88)</p> <p>(31) Priority Application Number: 115,228</p> <p>(32) Priority Date: 30 October 1987 (30.10.87)</p> <p>(33) Priority Country: US</p> <p>(71) Applicant: LSI LOGIC CORPORATION [US/US]; 1551 McCarthy Boulevard, Milpitas, CA 95035 (US).</p> <p>(72) Inventors: LONG, Jon ; 256 Helen Way, Livermore, CA 94550 (US). SIDOROVSKY, Rachel, S. ; 1621 Danromas Way, San Jose, CA 95129 (US).</p> <p>(74) Agents: MacPHERSON, Alan, H. et al.; Skjerven, Morrill, MacPherson, Franklin & Friel, 25 Metro Drive, Suite 700, San Jose, CA 95110 (US).</p>	<p>(81) Designated States: AT (European patent), BE (European patent), CH (European patent), DE (European patent), FR (European patent), GB (European patent), IT (European patent), JP, KR, LU (European patent), NL (European patent), SE (European patent).</p> <p>Published With international search report. Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.</p>	

(54) Title: METHOD AND MEANS OF FABRICATING A SEMICONDUCTOR DEVICE PACKAGE



(57) Abstract

A semiconductor device assembly is made without a molded package by using a tape having a patterned insulating layer (12) and a conductive layer (14) joined thereto. A semiconductor die (24) is seated on the conductive layer (14) and electrically connected to leads of the patterned conductive layer (14). A body frame (40) is positioned around the die (24) and electrical leads and connections, and an encapsulant material (28) is distributed over the frame (40) and within the frame (40) over the die (24) and electrical leads and connections.

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METHOD AND MEANS OF FABRICATING A
SEMICONDUCTOR DEVICE PACKAGE

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CROSS-REFERENCE TO COPENDING U.S. PATENT APPLICATION

U.S. Patent Application Serial No. 07/008,208, filed January 28, 1987, and assigned to the same assignee, discloses a support assembly for integrated circuits. U.S. Patent Application Serial No. 07/049,641, filed May 13, 1987, and assigned to the same assignee, discloses an integrated circuit device package wherein an insulating layer is etched and patterned. The subject matters of the copending patent applications are incorporated herein for reference.

15

FIELD OF THE INVENTION

This invention relates to a method and means of fabricating a semiconductor device package.

20

BACKGROUND OF THE INVENTION

Prior art semiconductor device packages are fabricated in a sandwich mold configuration wherein the semiconductor device is encapsulated forming a package on both sides of the die. When the package is cooled after the molding process, the larger molded package tends to curl, which results in a defective or unusable device. Also, if the package has any minute openings or cracks that allow moisture to penetrate to the elements of the semiconductor device, delamination of the semiconductor die can occur, which will render the device defective, or will cause the device to have a reduced operating life. Furthermore, the use of a mold to construct the package increases the height and area of the package significantly.

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A composite package assembly, such as disclosed in the
aforementioned copending patent applications, is formed with
a rigid lead frame and a thin flexible tape-like structure.
The tape-like structure is configured with lead fingers that
are connected to leads of the lead frame. The semiconductor
assembly, which includes bond wires, is encapsulated using a
two section mold that requires a number of molding steps to
encompass the semiconductor device with the lead frame,
tape-like structure, bond wires and conductive leads.

Conventional semiconductor molded packages which are
standard in the semiconductor industry accommodate up to 160
conductive leads, which typically are spaced between 50 and
25 milli-inches from center to center. As the number of
leads are increased, the number of bond wires that connect
to the leads are increased accordingly. The increase in
bond wires results in a larger package.

A major objective of the semiconductor industry is to
make semiconductor devices with more conductive leads and
yet to have a more compact package. With a more compact
package, semiconductor die with more die pads can be used,
which requires closer spacing of the leads of the
semiconductor assembly. As a result, higher circuit
operating speeds can be realized with improved operating
reliability.

SUMMARY OF THE INVENTION

An object of this invention is to provide a novel and
improved semiconductor package which eliminates the need for
a molding process to form a plastic package body.

Another object of this invention is to provide a
semiconductor package in which wire bonding can be
eliminated.

Another object is to provide a semiconductor package
that affords a relatively large number of conductive leads
and external pins.

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A further object is to provide a semiconductor package that affords a high degree of protection from moisture.

In accordance with this invention, a tape is formed of a patterned insulating layer and a conductive layer that is joined to the insulating layer. A semiconductor die is attached to a pad on one surface of the tape and electrically connected to leads of the conductive layer. An insulating coat is dispensed over the die and wire leads. At the surface opposite to the die attach pad, a tape element is adhered to the conductive layer. A package frame or body frame is joined to the tape surrounding the semiconductor die and electrical connections and leads. The body frame serves to contain an encapsulant that is distributed over the top of the body frame, the die and conductive wires and leads.

In one embodiment, conductive bumps in lieu of wire leads are used for electrical connection. Tab bonding is employed to join the bumps which are formed on the die and the conductive layer. As a result, the semiconductor device package is made more compact and accommodates an increased number of leads and external pins.

DESCRIPTION OF THE DRAWINGS

The invention will be described in greater detail with reference to the drawings in which:

Figure 1 is a sectional side view of a semiconductor assembly, in part, made in accordance with this invention;

Figure 2 depicts the attachment of a semiconductor die to the partial assembly of Figure 1;

Figure 3 illustrates the wire bonding of the die to conductive lead fingers of the assembly;

Figure 4 shows the application of a protective coating over the semiconductor die and bond wires;

Figure 5 illustrates the partial assembly, turned upside down, for attaching an aligned backside tape, in

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accordance with this invention;

Figure 6 illustrates the joinder of a frame body to the assembly;

Figure 7 is a sectional view of a semiconductor device
5 package, made in accordance with this invention;

Figure 8 is a top plan view, partly opened, depicting a semiconductor device package, made in accordance with this invention;

Figure 9 is a sectional view of a semiconductor device
10 package, using tape automated bonding (TAB), to join and electrically connect the semiconductor die to the patterned conductive layer by means of conductive bumps; and

Figure 10 is an exploded view of the semiconductor device package of this invention.

15 Similar numerals refer to similar elements throughout the drawing.

DETAILED DESCRIPTION OF THE INVENTION

With reference to Fig. 1, in an implementation of the
20 invention, a wire bondable tape 10 is formed of a patterned insulating layer 12 made of Kapton (trademark of DuPont), for example, and a gold plate layer 14 that is joined to the Kapton layer. The gold plate layer is about 30-40 microinches thick, by way of example. A thin copper film 16
25 is sputtered onto the Kapton layer 12 prior to deposition of the gold layer 14 to provide conductivity to the layer 12 and to facilitate adhesion of the gold to the Kapton material. The layer 12 is etched and patterned with cavities for down bonding, as disclosed in copending U.S. Patent
30 Application Serial No. 07/049,641, filed on May 13, 1987.

The patterned wire bondable tape is positioned in a fixture 18, to provide flatness to the tape. Die attach epoxy 22, such as Amicon 990C (trademark of Amicon) is spread on a die attach pad 20 formed on one surface of the
35 wire bondable tape. A semiconductor die 24 is then aligned

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and placed on the die attach epoxy as illustrated in Fig. 2. The die attached unit is placed in an oven for curing at a maximum cure temperature of about 150°C for a maximum cure time of about one hour.

5 The cured die attached unit is placed on a vacuum heater block (such as disclosed in copending U.S. Patent Application Serial Number 07/043,894 filed April 29, 1987) to hold the unit rigid and at a temperature of about 200°C. Then the unit is wire bonded thermosonically with
10 gold wires 26 as shown in Fig. 3 to make electrical connection between the die 24 and lead fingers or conductive elements of the patterned gold layer 14. A silicone gel 28, such as Dow Corning Q1-4939, having a 1 to 10 mixing ratio of curing agent to its base is then applied as a die coat
15 over the die, first starting in the corners and then distributing the gel in the middle of the die. The gel is permitted to flow to cover the die and wires (see Fig. 4) but is contained within a prescribed area, as disclosed in the aforementioned copending patent application Serial No.
20 07/049,641. The die coated unit is then cured in an oven at about 150°C for about one hour.

After the die coat cure, the unit is turned upside down and is positioned within an alignment fixture 30 as depicted in Fig. 5. The fixture 18 is used to protect the die, wires
25 and die coat from damage. A tape element 32 that has an adhesive 34 on one surface is set down on the lower surface or backside of the conductive layer 14 which is part of the wire bondable tape 10. A metal block 36 that has been preheated on a hot plate at a temperature in the range of
30 100-150°C approximately is brought into contact with the tape element 32 for about 1 to 1.5 minutes to cause the adhesive 34 to flow and adhere to the backside of the conductive element 14, while the tape 10 is maintained in alignment. The fixture 30 is replaced by a fixture (not
35 shown) having a wider window to ensure that the adhesive 34

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will not stick to the fixture 30 during the curing process that follows. To accomplish the curing, the unit is placed in an oven with the die side or upper surface of the tape 10 facing down for about 1/2 hours at approximately 150°C.

5 In accordance with this invention, a package frame or body frame 40, preferably made of a polymer material such as Ryton (trademark of Phillips Chemical Co) is joined to the cured unit by means of an epoxy adhesive 42, which may be a B-stage adhesive such as RT-4B (trademark of RJR Polymers).
10 The unit is inserted into a fixture or tray 44, as shown in Fig. 6 with the die facing up. An insert 46 is positioned on top of the unit, and an alignment fixture 48 is located on top of the insert. While the unit is maintained at a temperature between 120-150°C, the body frame 40 is placed
15 into the alignment fixture 48 so that the adhesive 42 makes contact with the gold plate layer 14 and the tape element 32. A slight force is applied to the top perimeter of the frame by means of a block 50, as shown in Fig. 6. The pressure is applied to the frame for about 15-30 seconds.
20 The unit with the attached frame is then cured at about 150°C for approximately one hour.

After the unit with the body frame cures, an electronic grade epoxy material 52, such as Hysol CNB 405-12 (trademark of Hysol) is used to encapsulate the device, while the
25 temperature of the unit is maintained at about 50-70°C. The epoxy is distributed by a dispensing needle, for example, in a circular motion, starting at the perimeter or corners inside the body frame and moving to the center of the die area. The epoxy is made to flow evenly so that a substantially flat surface results and air bubbles are eliminated.
30 The epoxy effectively encapsulates the top of the body frame and the elements contained within the frame, as shown in Fig. 7. The epoxy encapsulant is then cured by placing the unit in an oven for 2-4 hours at a temperature
35 between 130°C to 150°C.

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In the top plan view of Fig. 8, the novel semiconductor device package of this invention, the relationship of the body frame 40 to the patterned Kapton layer 12 is shown. Sprocket holes 56 are provided with the wire bondable tape 10 to aid in the automated processing of the tape. Bond fingers 58 couple the bond wires 26 to outer lead fingers to enable electrical connection to external connections or pins 60, as disclosed in the referenced copending applications.

In another embodiment of the invention, conductive bumps 54 are employed in lieu of bond wires 26, to provide a conductive path from the die pad 20 to the conductive layer 14, as illustrated in Fig. 9. The bumps, which may be made of gold, copper or solder, are formed and joined by a tape automated bonding (TAB) process, which is well known in the art. The use of the bumps reduces the space required for the bond wires. By virtue of the elimination of bond wires, the assembly provides a more compact package and allows a relatively high lead count, because there is no physical space limitation by a molded enclosure as found in the prior art.

With reference to Fig. 10, the exploded view of the semiconductor device package of this invention shows the body frame 40, which has a vertical dimension, which may be approximately 60 milli-inches for example, and the epoxy encapsulant body 52 as they relate to the wire bondable tape. The assembly does not include a molded package surrounding the semiconductor elements and does not incorporate a conductive patterned lead frame which is part of the electrically conductive path. The body frame or package frame of this invention eliminates the need for molding a package around the semiconductor device and may be made of plastic or nonconductive material. The body frame is used to contain the epoxy encapsulant body which provides the desired protection to the components of the semiconductor device.

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Although the description herein is directed to the processing of a single unit, it should be understood that the process is applicable to produce a multiplicity of units simultaneously. Also, the invention is not limited to the materials and parameters specified herein and modifications may be made within the scope of the invention.

There has been disclosed a novel design for a semiconductor device package and a process for implementing the package design. The novel plastic package eliminates the need for a molded enclosure, is greatly reduced in height and overall area, and realizes improved electrical performance and reliability. There is virtually no problem of delamination of the insulating area, which is Kapton for example, from the conductive layer, with a conductive film therebetween. Moisture penetration is effectively minimized. Also there is no problem of die surface corrosion.

CLAIMS

What is claimed is:

- 5 1. A semiconductor device package comprising:
a tape including a patterned insulating layer and
a conductive layer, said conductive layer being joined
to said insulating layer;
a semiconductor die secured to one surface of said
10 tape;
an insulating element joined to said conductive
layer;
means for electrically coupling said semiconductor
die to said conductive layer;
15 a body frame joined to said conductive layer and
positioned about said semiconductor die and said
electrical coupling means; and
an encapsulant body disposed over said frame and
within said frame over said die and said electrical
20 coupling means.
2. A semiconductor device package as in Claim 1,
including a conductive film disposed between said patterned
insulating layer and said conductive layer.
- 25 3. A semiconductor device package as in Claim 2,
wherein said conductive film is formed from sputtered
copper.
- 30 4. A semiconductor device package as in Claim 1,
wherein said insulating layer is made of a flexible
material.
- 35 5. A semiconductor device package as in Claim 3,
wherein said insulating layer is made of Kapton.

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6. A semiconductor device package as in Claim 1, wherein said conductive layer is made of gold plate.

5 7. A semiconductor device package as in Claim 1, including an insulating element joined to the backside of said conductive layer.

10 8. A semiconductor device package as in Claim 1, wherein said coupling means comprise bond wires.

9. A semiconductor device package as in Claim 7, including a silicon gel disposed over said die and said bond wires.

15 10. A semiconductor device package as in Claim 1, including bond lead fingers coupled to said bond wires, and conductive pins coupled to said bond lead fingers for connection to external conductive leads.

20 11. A semiconductor device package as in Claim 1, wherein said electrical coupling means comprise conductive bumps.

25 12. A semiconductor device package as in Claim 10, wherein said insulating element is a backside element, and said body frame is connected to said backside element surrounding said conductive leads.

30 13. A semiconductor device package as in Claim 1, wherein said body frame has a height substantially greater than the thickness of said patterned insulating layer.

14. A process of making a semiconductor device package comprising the steps of:

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forming a patterned wire bondable tape by sputtering a conductive film on an insulating layer;

etching the insulating layer and conductive film to define a pattern of conductive leads;

5 depositing a patterned conductive layer on said conductive film;

attaching a semiconductor die to said wire bondable tape;

10 forming electrical connections between said die and said conductive layer;

joining an insulating element to the backside of said conductive layer;

depositing a protective insulating coating over said die and electrical connections;

15 attaching a body frame to the upper surface of said conductive layer and insulating element, surrounding said die, electrical connections and coating; and

20 encapsulating said body frame, coating, die and electrical connections with an insulating material.

15. A process as in Claim 14, wherein said die is attached to said tape by a die attach epoxy and cured at a temperature of about 150°C for one hour or less.

25 16. A process as in Claim 14, including the step of forming said electrical connections are formed by thermosonically bonding wires between said die pads to conductive leads of said patterned conductive layer.

30 17. A process as in Claim 14, wherein said step of depositing a protective coating comprises applying a silicone gel to flow over said die and electrical connections and curing the gel coating.

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18. A process as in Claim 14, including the step of causing a body frame adhesive to flow to said insulating element on said conductive leads.

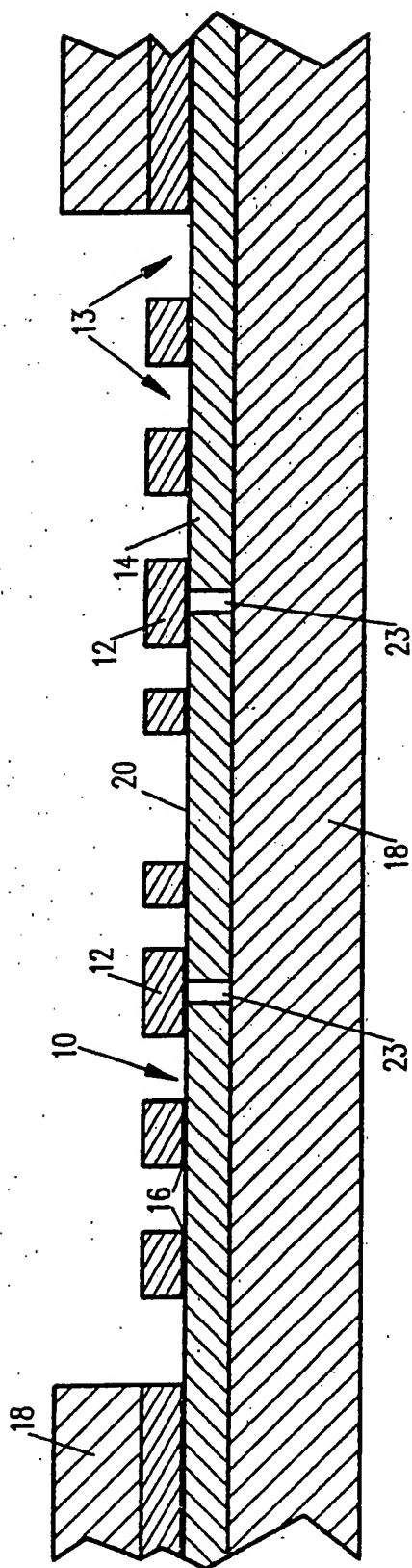


FIG. 1

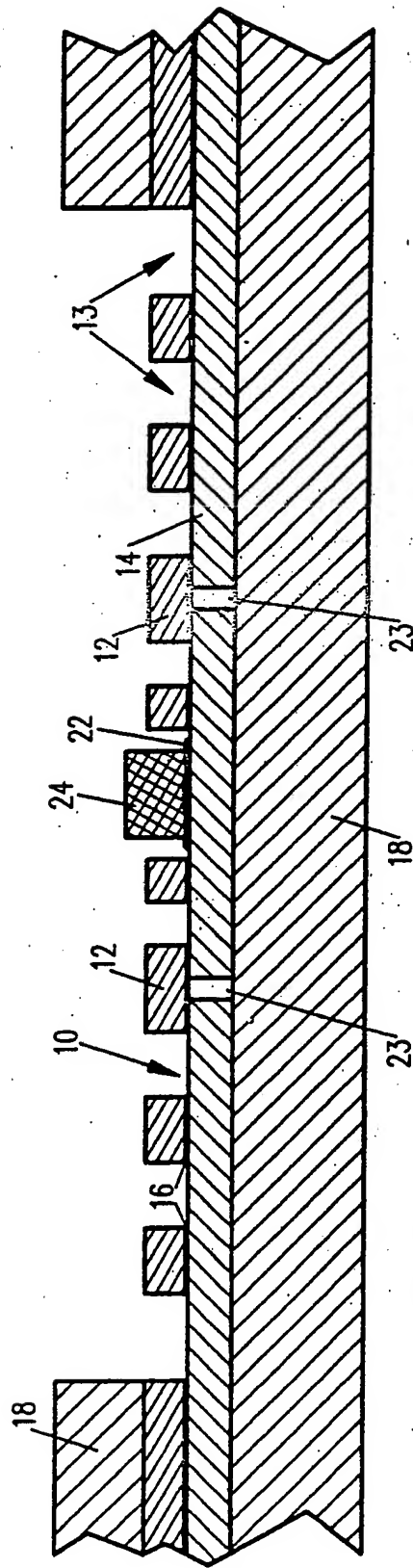


FIG. 2

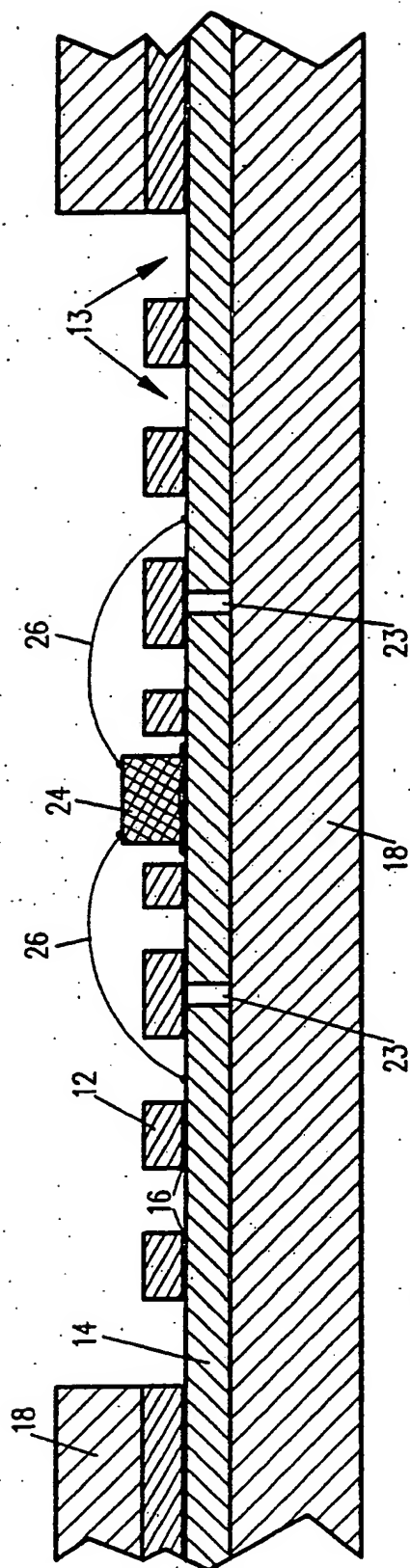


FIG. 3

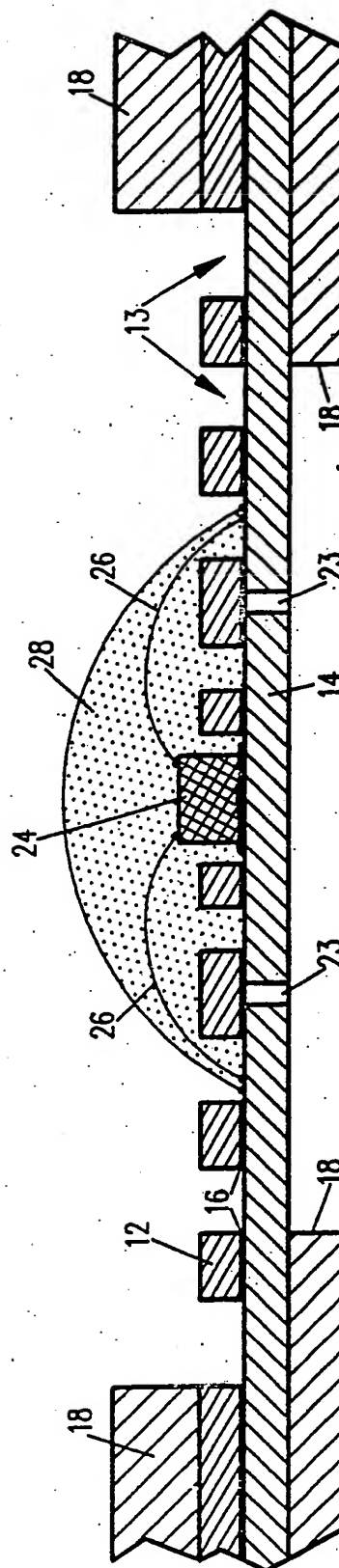


FIG. 4

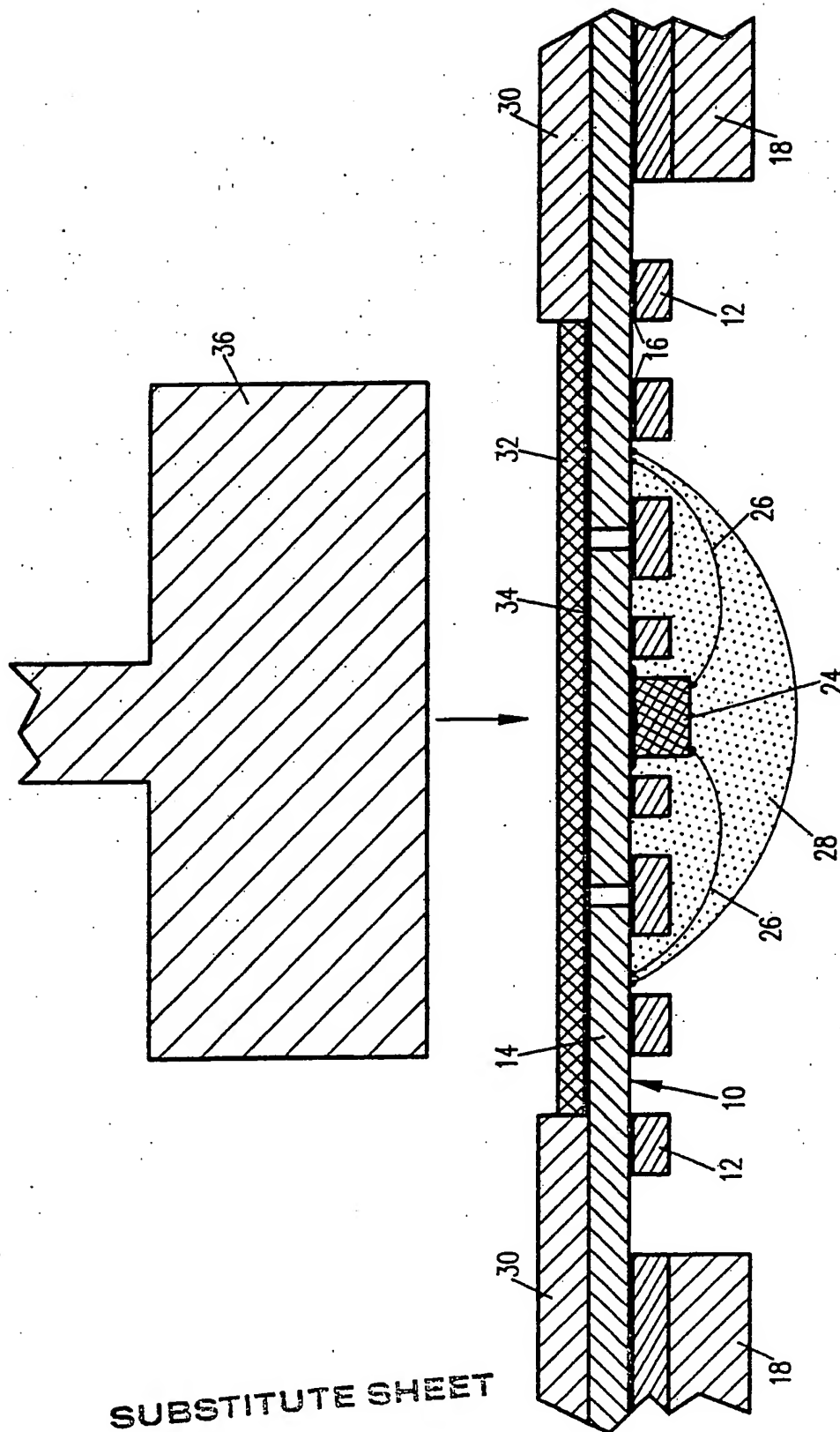


FIG. 5

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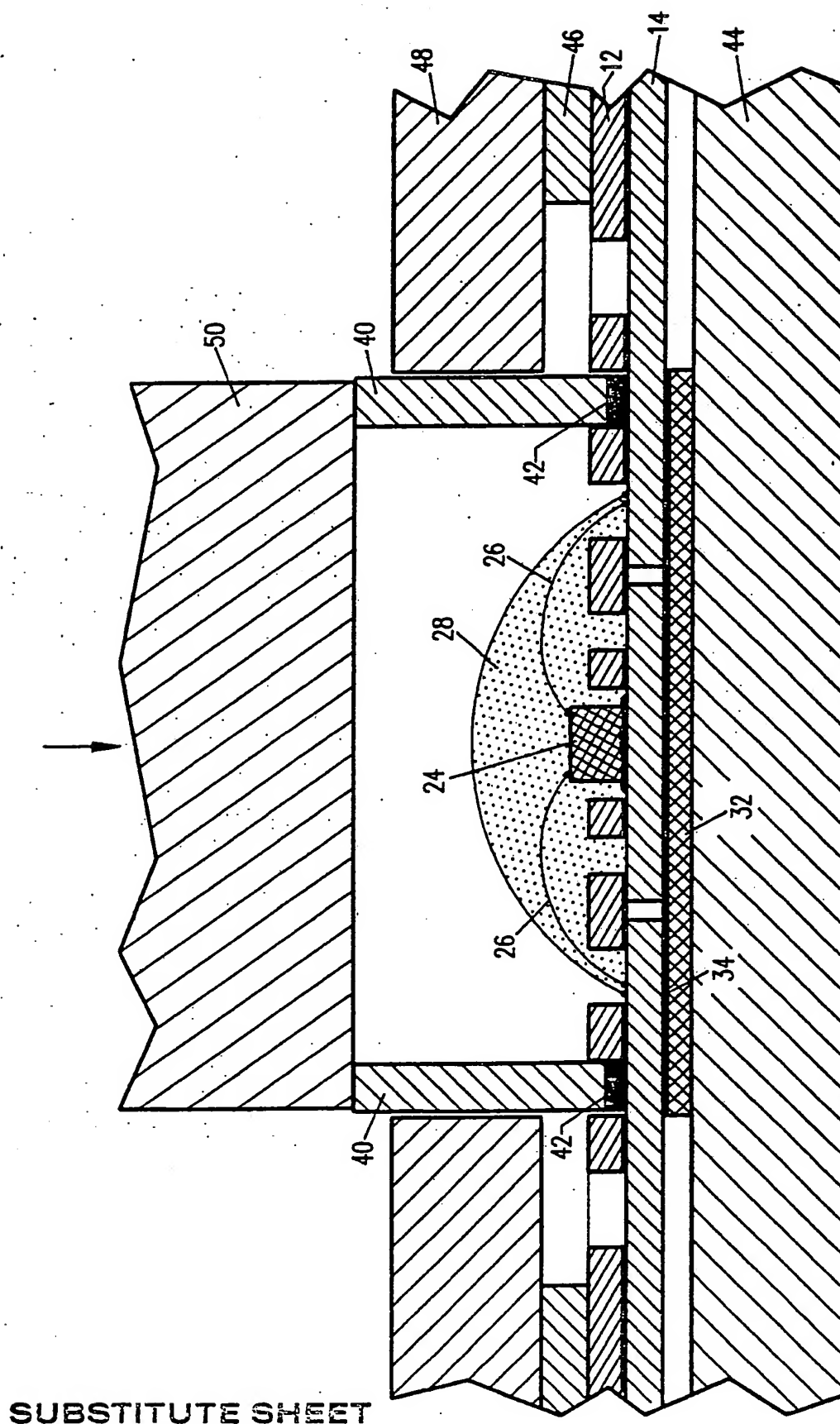


FIG. 6

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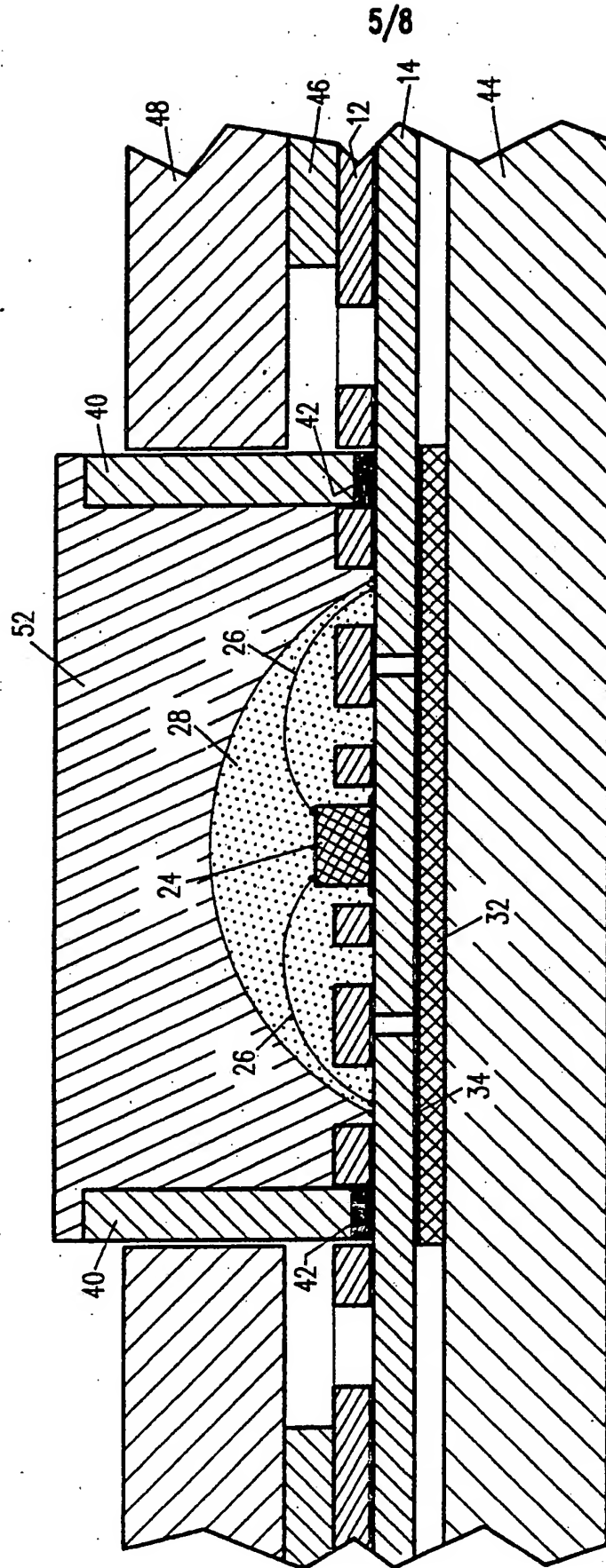


FIG. 7

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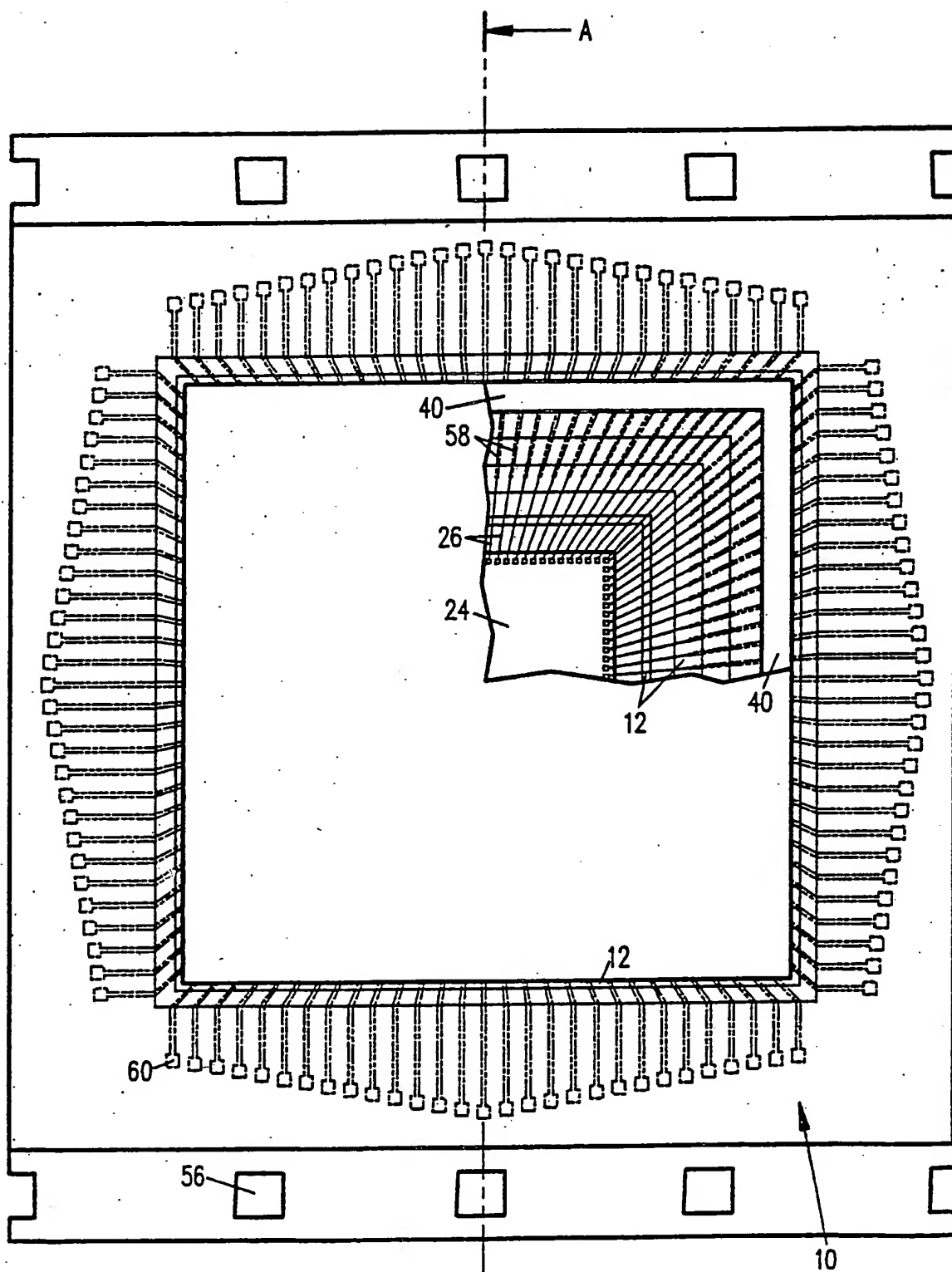


FIG. 8

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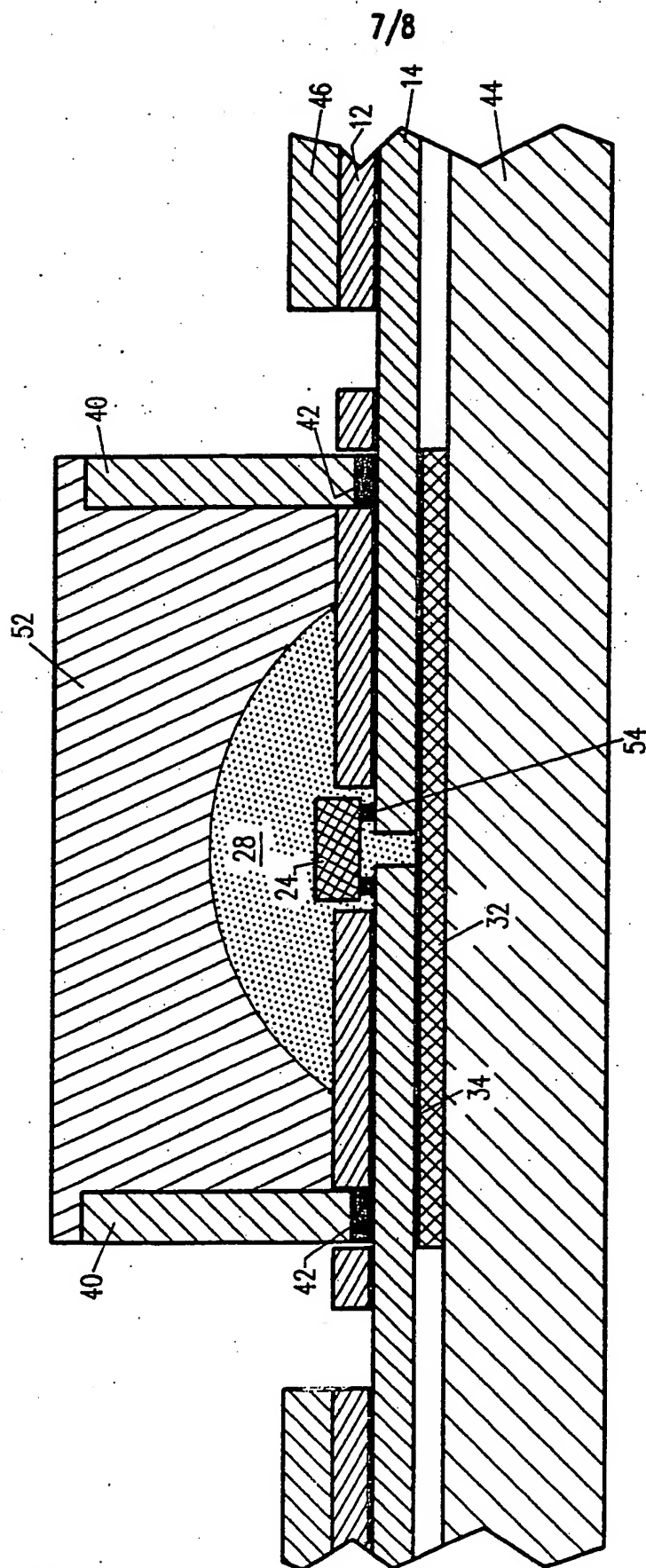


FIG. 9

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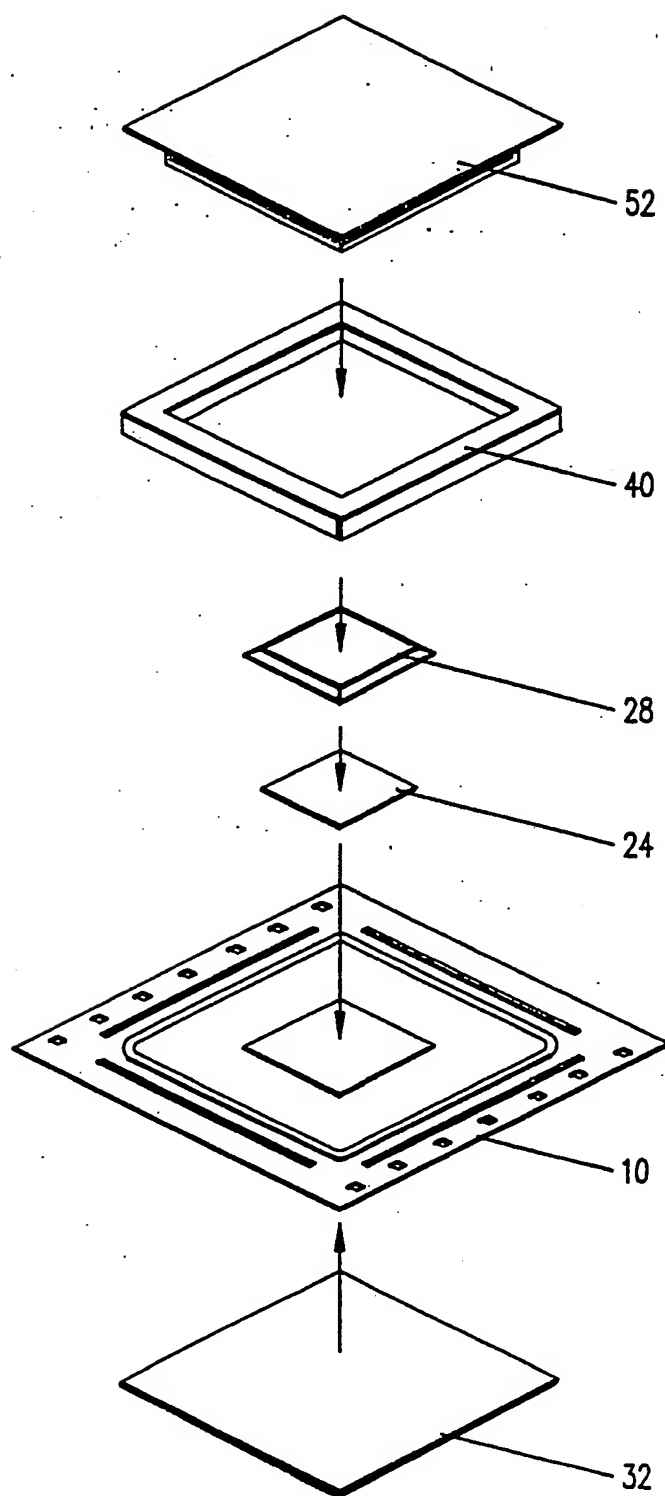


FIG. 10

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INTERNATIONAL SEARCH REPORT

International Application No. PCT/US 88/03790

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) ⁶ According to International Patent Classification (IPC) or to both National Classification and IPC: IPC ⁴ : H01L 23/48, H01L 29/52 U.S. CL. 357/68,69,70,80;437/195,206,207,217,224						
II. FIELDS SEARCHED <div style="text-align: center; border-top: 1px solid black; border-bottom: 1px solid black;">Minimum Documentation Searched ⁷</div> <table style="width: 100%; border-collapse: collapse;"> <tr> <th style="width: 20%; text-align: left; border-bottom: 1px solid black;">Classification System</th> <th style="text-align: left; border-bottom: 1px solid black;">Classification Symbols</th> </tr> <tr> <td style="border: 1px solid black; padding: 5px;">U.S. CL.</td> <td style="border: 1px solid black; padding: 5px;">357/68,69,70,80 437/195,206,207,217,224</td> </tr> </table> <div style="text-align: center; border-top: 1px solid black; border-bottom: 1px solid black;">Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched ⁸</div>			Classification System	Classification Symbols	U.S. CL.	357/68,69,70,80 437/195,206,207,217,224
Classification System	Classification Symbols					
U.S. CL.	357/68,69,70,80 437/195,206,207,217,224					
III. DOCUMENTS CONSIDERED TO BE RELEVANT ⁹						
Category *	Citation of Document, ¹¹ with indication, where appropriate, of the relevant passages ¹²	Relevant to Claim No. ¹³				
Y	US, A 4,380,042 ANGELUCCI, Sr. ET AL., 12 April 1983 (12.04.83) (Note entire document)	1-18				
Y	US, A 3,711,625 DUPUIS, 16 January 1973 (16.01.73) (Note Figure 1 and 2)	1-18				
Y	US, A 4,218,701 SHIRASAKI 19 August 1980 (19.08.80) (Note entire document)	1-18				
Y	US, A 4,089,733 ZIMMERMAN 16 May 1978 (16.05.78) (Note Figure 4)	1-14				
A,P	US, A 4,711,688 PIENIMAA 08 December 1987 (08.12.87) (Note Figure 3)	1-18				
<div style="display: flex; justify-content: space-between;"> <div style="width: 45%;"> <p>¹⁰ Special categories of cited documents:</p> <p>"A" document defining the general state of the art which is not considered to be of particular relevance</p> <p>"E" earlier document but published on or after the international filing date</p> <p>"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)</p> <p>"O" document referring to an oral disclosure, use, exhibition or other means</p> <p>"P" document published prior to the international filing date but later than the priority date claimed</p> </div> <div style="width: 45%;"> <p>"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention</p> <p>"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step</p> <p>"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.</p> <p>"&" document member of the same patent family</p> </div> </div>						
IV. CERTIFICATION						
Date of the Actual Completion of the International Search 24 January 1989 (24.01.89)		Date of Mailing of this International Search Report <div style="text-align: center; font-size: 1.2em; font-weight: bold;">07 MAR 1989</div>				
International Searching Authority ISA/US		Signature of Authorized Officer Michael B. Singleton				